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APPENDEX II 1.131 DECLARATION 7 pages

M3: Motorola Mismatch Calculator

- Mismatch is a leading cause of yield loss and a determining factor of circuit performance in analog, mixed-signal ICs.
- Motorola has developed a new mismatch model that accounts for variations in physical process parameters and is accurate over geometry and bias.
- The designer need quick, easy access to the new model.
- The model is complex and automation is required.

$$\sigma^2_{Id} = \sum_{J} (\partial I_d / \partial p_j)^2 \sigma^2_{pj}$$

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Prior Art

- Prior art based on the simplistic Pelgrom model.
  - P. G. Drennan, C. C. McAndrew "A Comprehensive MOSFET Mismatch Model," 1999 IEEE IEDM.
- Does not have a proper physical foundation and has gross errors in mismatch prediction.
- Prior art can't handle non-traditional devices such as graded channel (GCMOS & halo) and power MOSFETs.
- Inferior commercial tool is available from BTA Technology.

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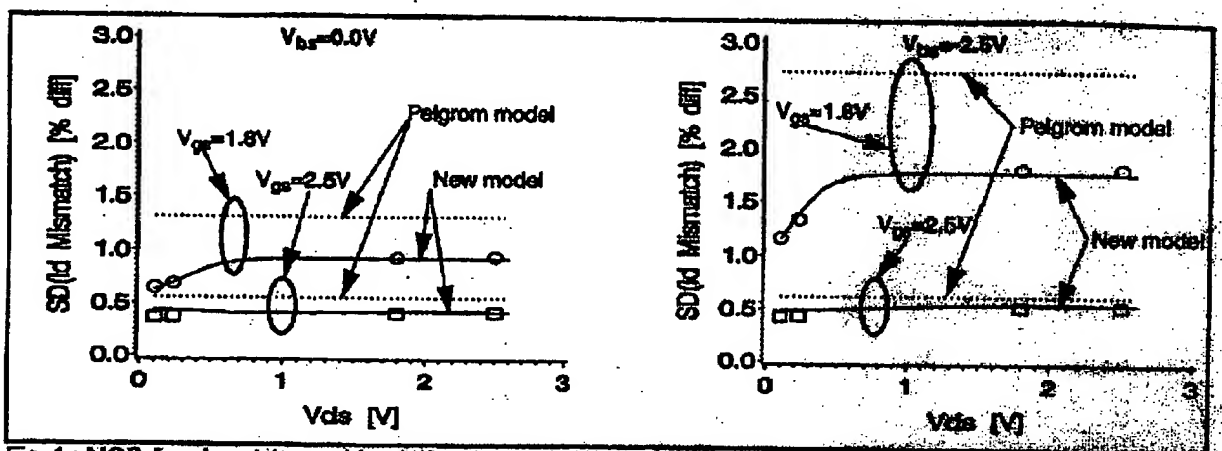

Fig. 1 nMOS I_d mismatch over bias, W/L=7/0.56μm. Circles are data for V_{gs}=1.8V and squares are for V_{gs}=2.5V.

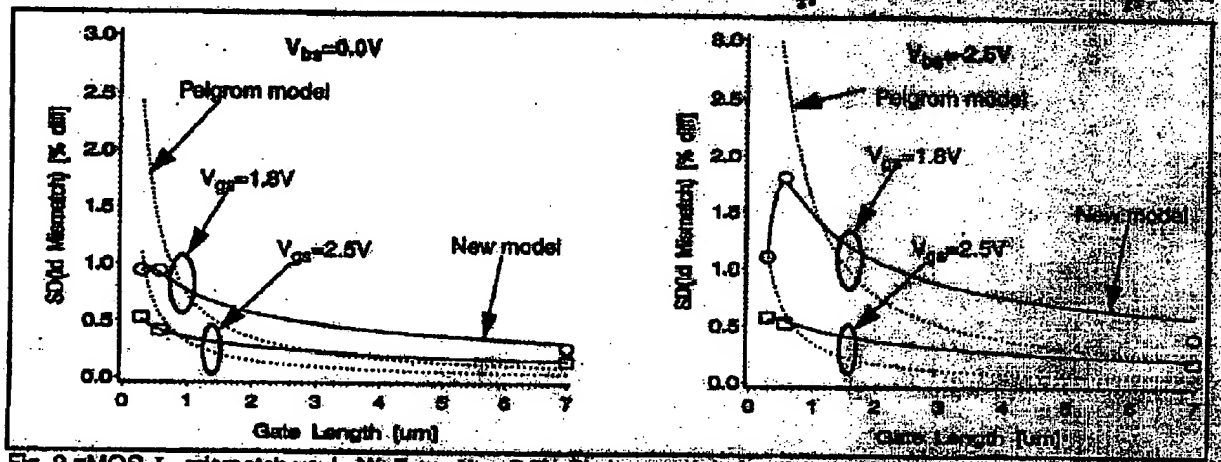

Fig. 2 nMOS I_d mismatch vs. L, W=7μm, V_{ds}=2.5V. Circles are data for V_{gs}=1.8V and squares are for V_{gs}=2.5V.

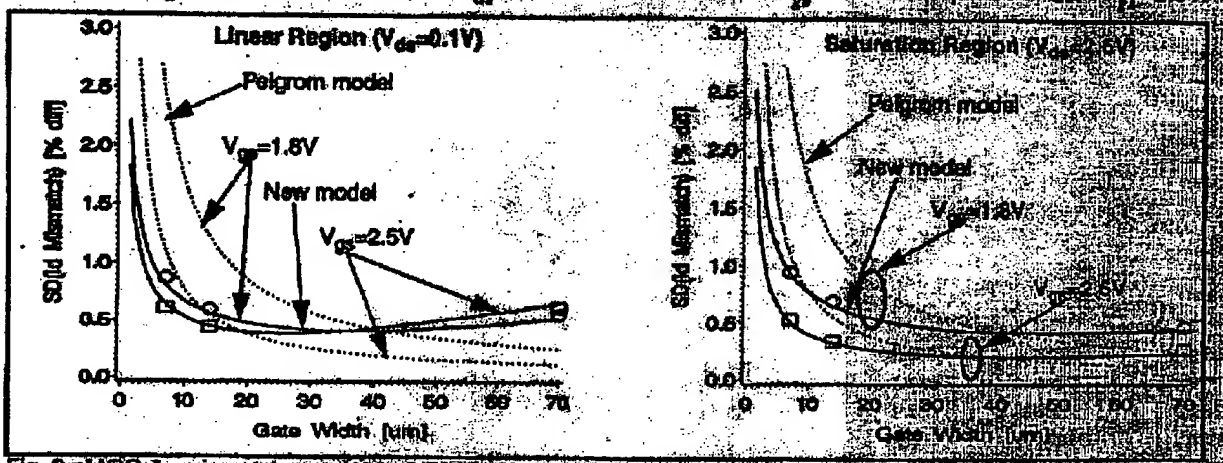

Fig. 3 nMOS I_d mismatch over W, L=0.56μm, V_{bs}=0.0V. Circles are data for V_{gs}=1.8V and squares are for V_{gs}=2.5V.

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M3: Proposed Solution

- Automate the Motorola Mismatch Model in the form of a web-based tool
- Three different solution types
  - Current Mirror (for designers)
  - Differential Pair (for designers)
  - Voltage Driven (for technology developers)
- Make the tool readily available throughout Motorola and only to Motorola
- Perform single mismatch predictions
- Perform multiple mismatch predictions by allowing the designer to sweep over bias and geometry

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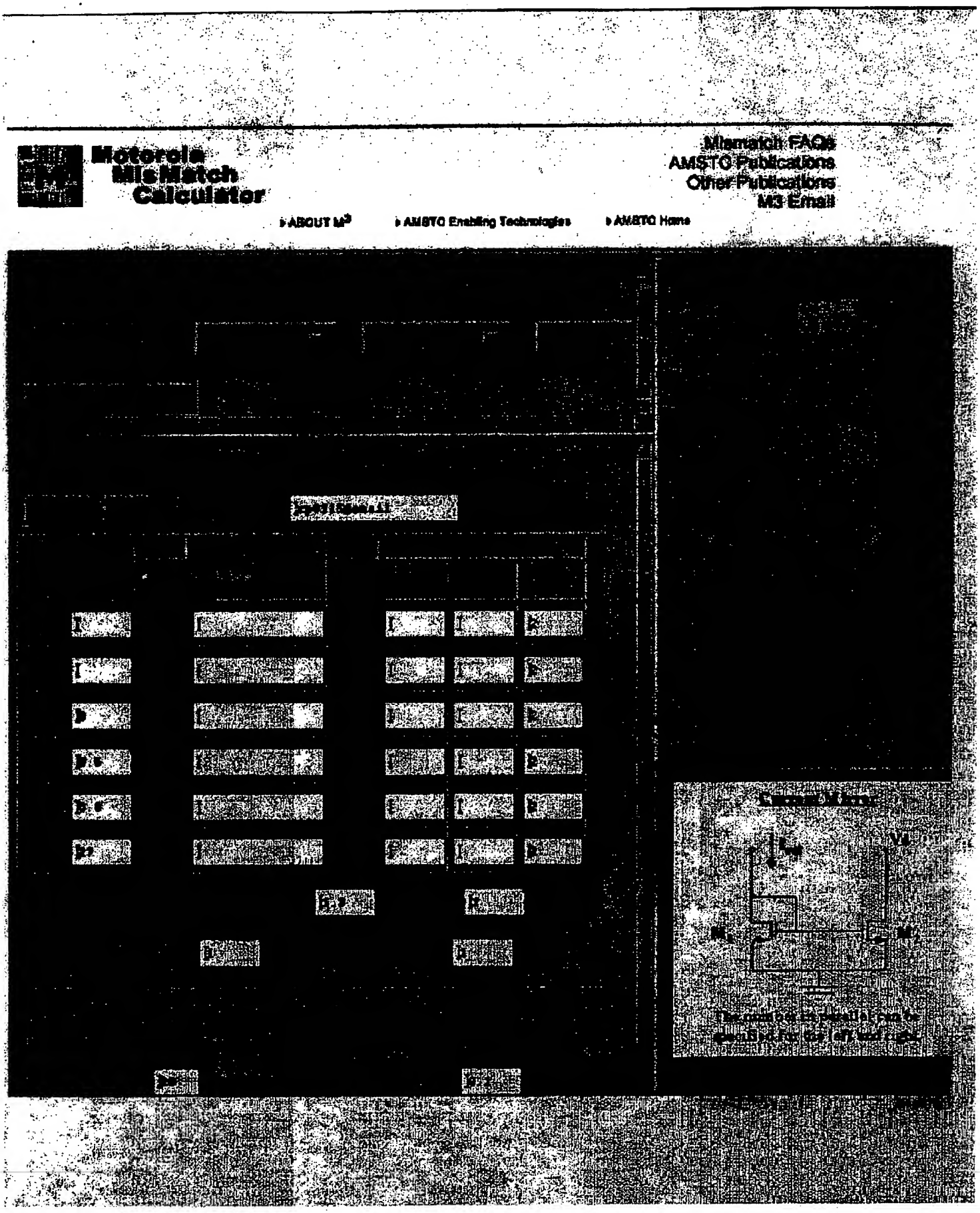
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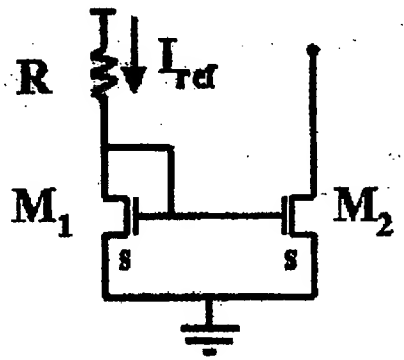
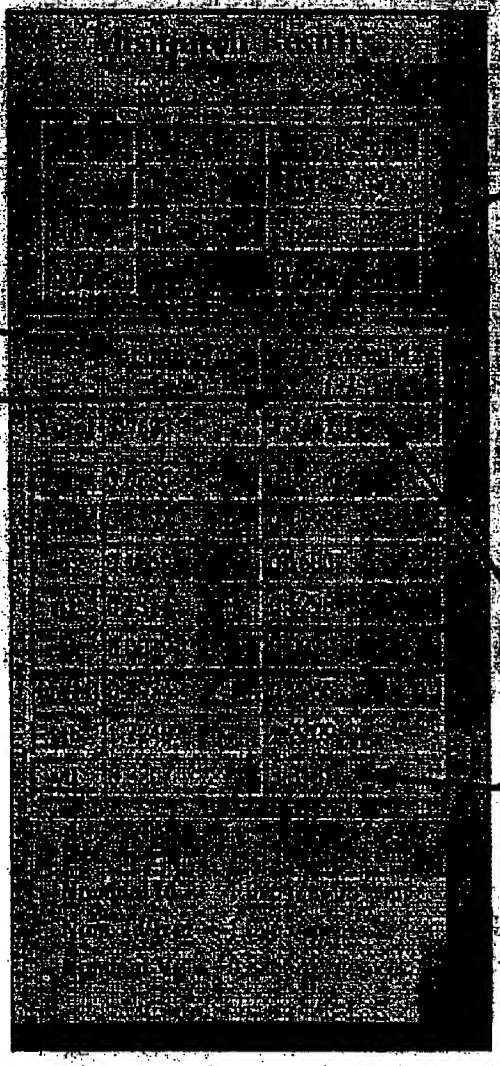
Sample output

Data Entered into interface

Two Outputs
- **Total Mismatch (%)**
- **Without go**
  Vd2 = Vg





Contributions to Mismatch
- **Root Sum of Squares, add variances, not standard deviations!**
- **vtl:Accounts for change in flat band voltage as a function of gate length**

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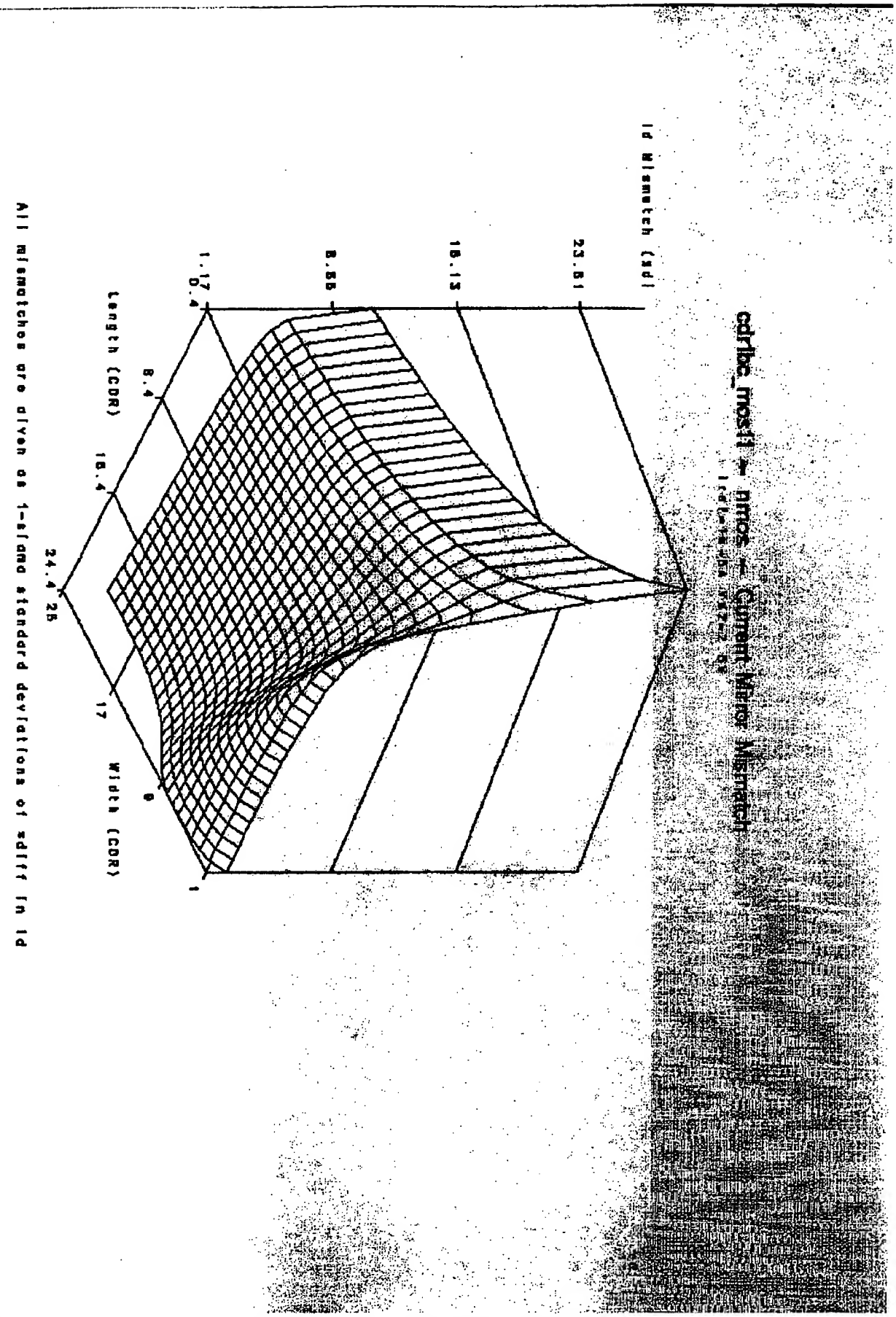
All mismatches are given as 1-sigma standard deviations of sdiff in id
Length (CDR)
Width (CDR)
Id Mismatch (sd)
cdrlbc_mos11 - nmos - Current Mirror Mismatch

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